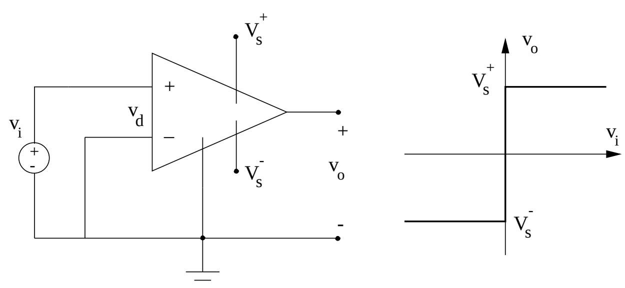
Comparators and Bistable Circuits

Analog-to-Digital (A/D or ADC) and Digital-to-Analog (D/A or DAC) circuits are in wide use today because of the need to translate analog signal to digital format for processing by microprocessors and translate the output of microprocessors (digital signal) to analog signal to drive loads. The heart of most ADC circuit is the "comparator" (see Rizonni Chap. 14 for some examples of ADC). A comparator compares the value of input signal to a reference voltage. If the input signal voltage is larger than the reference voltage, comparator output will be in a set voltage (for example, V^+, for a "HIGH" or "ON" state). If the input signal voltage is smaller than the reference voltage, comparator output will be in a different, yet set voltage (for example, V^-, for a "LOW" or "OFF" state).

An example of a comparator circuit using an "ideal" OpAmp is show below. Since the open-loop gain of the ideal OpAmp is infinite, we have:

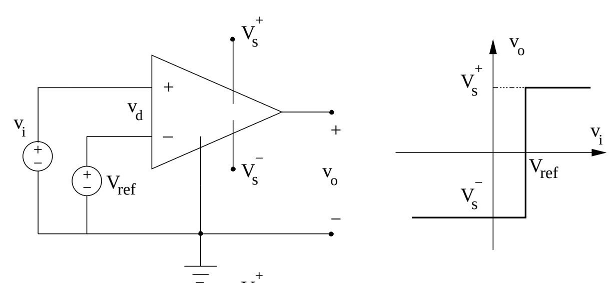
$$\text{if} \quad v_d = v_i > 0 \quad \rightarrow \quad v_o = A v_i \gg v_s^+ \quad \rightarrow \quad v_o = v_s^+$$
$$\text{if} \quad v_d = v_i < 0 \quad \rightarrow \quad v_o = A v_i \ll v_s^- \quad \rightarrow \quad v_o = v_s^-$$

The OpAmp compares the input signal with the reference value of "zero" (tests if $v_i > 0$). If the result is positive, the OpAmp output will be "high" ($v_o = v_s^+$), if the result is negative, the OpAmp output will be "low" ($v_o = v_s^-$). We can, for example, set $v_s^+ = 5$ V and $v_s^- = 0$ to drive a 5-V digital logic circuit.



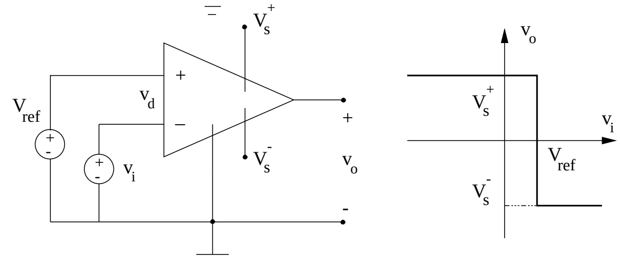
The above circuit can be generalized to any reference voltage (instead of zero):

$$v_i > v_{ref} \rightarrow v_d > 0 \quad \rightarrow \quad v_o = v_s^+$$
$$v_i < v_{ref} \rightarrow v_d < 0 \quad \rightarrow \quad v_o = v_s^-$$



Switching V_{ref} and v_i reverses the result of $v_i > 0$ test

$$v_i > v_{ref} \rightarrow v_d < 0 \quad \rightarrow \quad v_o = v_s^-$$
$$v_i < v_{ref} \rightarrow v_d > 0 \quad \rightarrow \quad v_o = v_s^+$$



While ordinary OpAmps (with no negative feedback) can be used as comparators, special purpose chips (variants of OpAmp circuits) are typically used in order to increase the switching speed between the two states of the comparator. Modern comparator chips have typical "slew-rates" a thousand time faster than comparable OpAmp chips. (Note that the term "slew-rate" is not usually used for comparator chips, rather terms such as "propagation delay" is often used in the literature.) In addition to faster response time, most of comparator chips have a low maximum output current (again to speed up to chip) because they drive digital logic circuits.

Alternatively, while the comparator chips are similar to OpAmps, in practice, they are never used in OpAmp circuits with negative feedback because of problems in the circuit stability (because their gain is not reduced at high frequency in order to keep switching speed high).

From the point of analytical circuit analysis, comparators and OpAmp chip are similar and ideal OpAmp circuit models can be used for both.

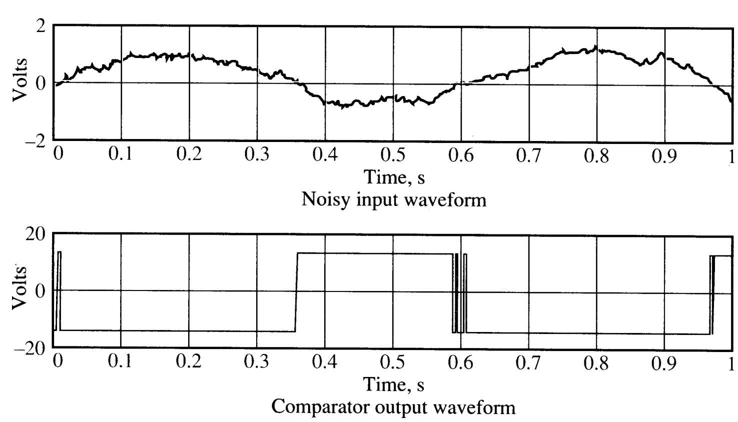
Bistable Circuits

There are two problems with the comparator circuit above:

(1) The gain of a practical comparator is not infinite. Output can be smaller than v_s^+ (or larger than $-v_s^-$) when v_i is close to V_{ref}. This can cause a major problem in some circuits which only expect the output voltage to be in one of two prescribed states. This is usually seen in slowly varying input signals, where the output may not switch rapidly from one voltage to another voltage.

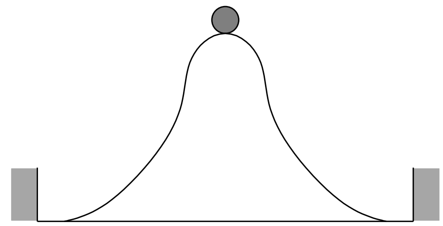
2) When the input signal is near the reference voltage, noise in the circuit can trigger the comparator to switch its state repeatedly as seen below. This is also a major problem in circuits where the input signal changes slowly.

Figure below shows the response a comparator circuit to slowly varying input which includes noise. Note the repeated switching of the comparator output at time of about 0.6 s.

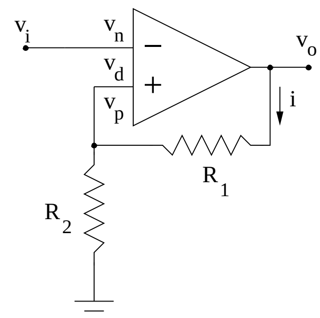


For a large number of application we need circuits which can have only two possible states (this solves concern 1 above). These circuits are called “Bistable” circuits.

A physical analogy for the operation of bistable circuits is shown. The ball cannot remain on the hill and it always drops to either side of the hill. The ball cannot even stay exactly at the top of hill for any length of time (a state of unstable equilibrium or a mesastate) as a small disturbance will forces to move down the hill to the either of two possible states.



Most amplifier circuits can be configured into a bistable circuit by using positive feedback. An example of such a circuit is shown. This circuit has positive feedback as the output of the OpAmp is connected to the non-inverting terminal of the OpAmp. As there is no negative feedback, the virtual short principle does not apply and $v_p \neq v_n$.

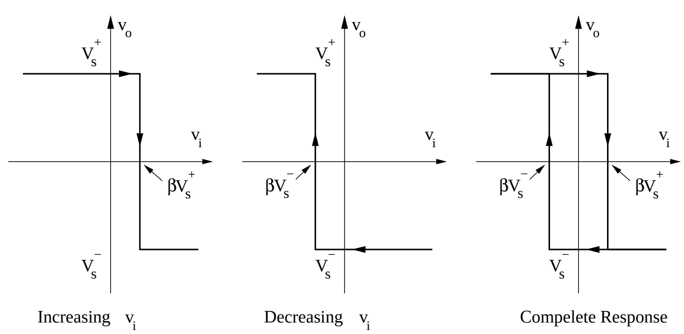


To solve the circuit, we note that because no current flows intro OpAmp (or comparator), R_1 and R_2 form a voltage divider:

$$v_p = \frac{R_2}{R_1 + R_2} v_o = \beta v_o \qquad \beta = \frac{R_2}{R_1 + R_2}$$

Let's assume that the circuit is in one of its two states, *e.g.*, $v_o = v_s^+$. Thus, $v_p = \beta v_s^+$. The circuit is in this state as long as $v_d = v_p - v_n > 0$, or since $v_n = v_i$, as long as $v_i < \beta v_s^+$. This value v_i is called that the higher threshold voltage. For the above circuit, $v_{th} = \beta v_s^+$. Suppose v_i starts increasing and at the some point it becomes slightly larger than v_{th} (no matter how small the difference is). In that case, $v_d = v_p - v_i$ becomes negative and forces the output of OpAmp to become negative. Then, $v_p = \beta v_o$ becomes negative making v_d much smaller (more negative), forcing the the output of OpAmp to become even more negative. This process continues until OpAmp becomes saturated and the output reaches its other state: $v_o = v_s^-$. This is contrast with a regular comparator (with no feedback) in which if v_d is very small, OpAmp will not be not saturated.

One can perform a similar analysis for the second state of circuit. Assuming $v_o = v_s^-$ and defining $v_{tl} = \beta v_s^-$, we find that the circuit remain in its state as long as $v_i > v_{tl}$ and switches to the other state when it falls below that value. Figure shows that transfer characteristics of the above bistable circuit.



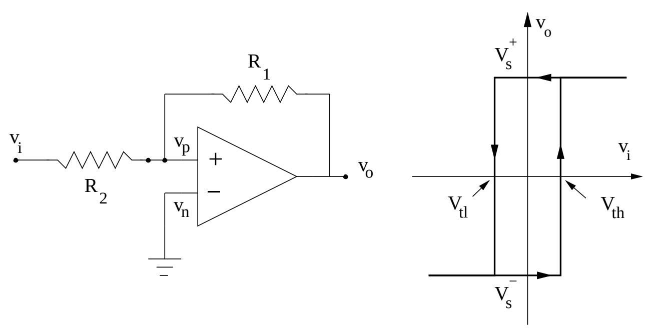
As can be seen from the transfer characteristics, this is a bistable circuit, the output can have only one of the two possible values. (While case of $v_i = 0$ and $v_o = 0$ is a solution to the above circuit, it is an unstable point, similar to the ball sitting exactly on the top of the hill, and any small amount of disturbance forces the circuit to reaches one of its two possible states.)

The transfer characteristics of the above bistable circuit has certain features:

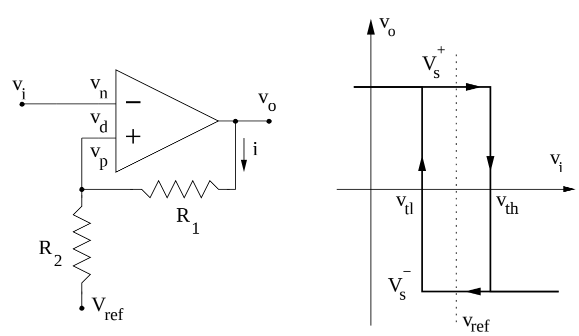
1. Hysteresis: As can be seen the circuit exhibits "hysteresis" – the circuit changes state at different values of v_i depending on whether v_i is decreasing or increasing. This "hysteresis" provides additional benefits in many applications. For example, because the state of the circuit depends on the value of previous trigger signal, the circuit exhibit memory! Indeed, bistable circuit is the basic memory element of digital systems. Hysteresis is also used to eliminate switching of comparators due to noise (see Schmidt Trigger circuit below)

2. Trigger: Suppose that $v_{tl} < v_i < v_{th}$. In this case, the circuit will be in one of its two possible states, suppose v_s^-. We can change the state of the circuit by applying an input signal $v_i > v_{th}$ to the circuit. This input pulse can be of a very short duration. As such, this input signal is referred to as a "trigger" signal. Alternatively, we can change the state of the circuit with v_s^+ by applying a negative pulse with $v_i < v_{tl}$.

3. Non-inverting vs Inverting Characteristics: The above circuit is a bistable circuit with an inverting transfer characteristics, *i.e.,* The output voltage is v_s^+ (positive) when the input is more negative than the negative trigger threshold and the output voltage is v_s^- (negative) when the input is larger than the positive trigger threshold. Small modification in the circuit leads to a bistable circuit with non-inverting transfer characteristics as is shown.



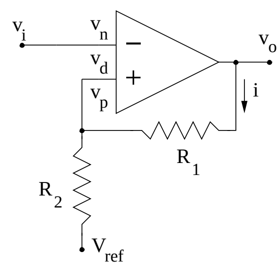
4. Location of Hysteresis Band: The center of the "hysteresis" band can also be located at a different voltage than zero by adding a reference voltage to the circuit as is shown.

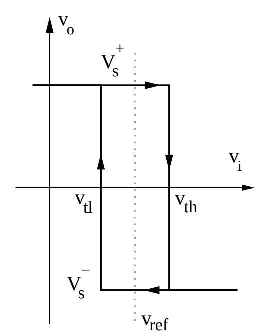


Application of the Bistable Circuit as a Comparator – Schmidt Trigger

The bistable circuit above can be used to resolve the two problems that we have identified for a comparator. 1) Because of the positive feedback, the output switches rapidly between the two states and is always one of the two values no matter how small the input signal is, and 2) The hysteresis characteristics can be used to eliminate switching of the comparator by the noise.

As an example, consider a common application of comparators. It is required to design a circuit that detects and counts how many times an input signal crosses zero. Such a circuit can be implemented with a comparator with a threshold value of 0 V. Suppose now that the input signal has a noise superimposed on it (a common occurrence). As such, when the input signal is near zero, the noise can cause several crossing of zero voltage without input signal ever crossing zero (or crossing once). If we have an idea of the peak-to-peak amplitude of the noise, we can design a bistable circuit with a hysteresis band which is slightly larger than the expected noise level. In that case, noise will never trigger the comparator.





Such a circuit is shown and is commonly called a Schmidt Trigger. The method of solution of the circuit (as with all bistable circuits) is as follows. Assume that we are in one of the possible two states for v_o. Compute v_d and find the range of v_i for which $v_d > 0$. As long as v_i remains in this range, the comparator state does not change. However, when v_i moves out of this range, v_d switches sign and comparator state changes. Before we start the analysis, we note:

$$v_d = v_p - v_n = v_p - v_i$$

$$i = \frac{v_o - V_{ref}}{R_1 + R_2}$$

$$v_p - V_{ref} = iR_2 = \frac{R_2}{R_1 + R_2}(v_o - V_{ref}) \quad \rightarrow \quad v_p = \frac{R_2}{R_1 + R_2}\, v_o + \frac{R_1}{R_1 + R_2}\, V_{ref}$$

<u>Case 1:</u> $v_o = v_s^+$ (requires $v_d > 0$). Then:

$$v_p = \frac{R_2}{R_1 + R_2}\, v_s^+ + \frac{R_1}{R_1 + R_2}\, V_{ref}$$

Since $v_d = v_p - v_i > 0$, the range of v_i for the Schmidt trigger to stay in its current state is $v_i < v_p$ (or v_{th} is v_p).

$$v_i < v_{th} = \frac{R_2}{R_1 + R_2}\, v_s^+ + \frac{R_1}{R_1 + R_2}\, V_{ref}$$

So as the comparator is in the high state and we increase v_i, comparator stays in that state until the condition of $v_i < v_{tl}$ is violated, as is shown in the transfer characteristic figure in the previous page (note direction of arrows).

Case 2: $v_o = v_s^-$ (requires $v_d < 0$). Then:

$$v_p = \frac{R_2}{R_1 + R_2} v_s^- + \frac{R_1}{R_1 + R_2} V_{ref}$$

Since $v_d = v_p - v_i < 0$, the range of v_i for the Schmidt trigger to stay in its current state is $v_i > v_p$ (or v_{tl} is v_p):

$$v_i > v_{tl} = \frac{R_2}{R_1 + R_2} v_s^- + \frac{R_1}{R_1 + R_2} V_{ref}$$

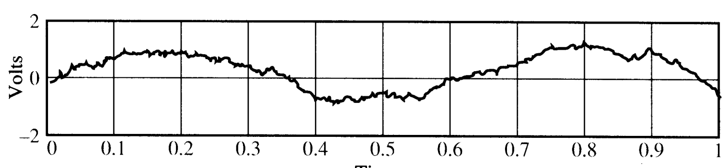
So as the comparator is in the low state and we decrease v_i, comparator stays in that state until the condition of $v_i > v_{tl}$is violated, as is shown in the transfer characteristic figure in the previous page (note direction of arrows).

The hysteresis region,

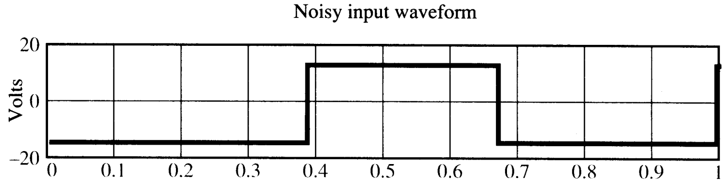
$$\frac{R_2}{R_1 + R_2} v_s^- + \frac{R_1}{R_1 + R_2} V_{ref} < v_i < \frac{R_2}{R_1 + R_2} v_s^+ + \frac{R_1}{R_1 + R_2} V_{ref}$$

is called the dead band. The input signal should pass completely through this band before the output of trigger switches from one state to another. The value of v_s^- and v_s^+ are chosen based on the desired value of the comparator output voltages. Value of V_{ref} sets the "average" switching input voltage as shown. Values of $R_2/(R_1 + R_2)$ are usually set based on the level of the noise in the circuit. Typically the width of the dead band is chosen to be slightly larger than the maximum expected peak-to-peak amplitude of the noise.

Figure below shows the response of the Schmidt trigger to the same noisy input as previous stage. Note that multiple triggering of the comparator by the noise has been eliminated.



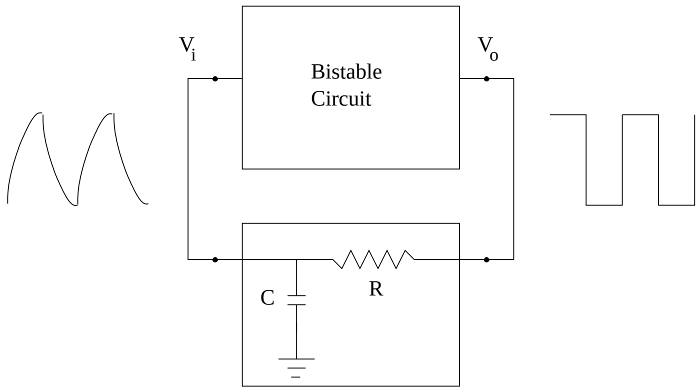
Noisy input waveform



Schmitt trigger output waveform

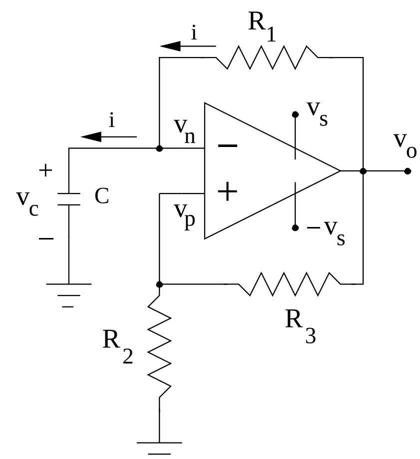
Waveform Generation with Bistable Circuits (Astable Multivibrator)

Square and triangular waveforms can be generated by adding a RC feedback loop to a bistable circuit as is shown below. As we will see, this circuit has no stable state and, as such, belongs to a class of circuit called astable multivibrators.



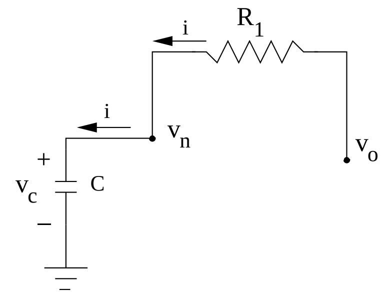
To see how this circuit works, let's assume that the bistable circuit is in one of its two states, suppose v_s^+. The capacitor is charged through resistor and the voltage across the capacitor moves toward v_s^+ with a time constant RC. The voltage across the capacitor is connected to the input the bistable circuit. Once, the voltage across the capacitor passes the threshold voltage, v_{th}, the bistable circuit is triggered and its output voltage drops to v_s^-. Now the capacitor discharges and its voltage drops toward v_s^- with the constant RC. When the voltage across the capacitor drops below v_{tl}, the bistable is triggered again and its states changes back to v_s^+. This switching back and forth continues and the output of the bistable circuit is a square wave.

An example of an astable multivibirator is a combination of a Schmidt trigger and an RC circuit. At first glance it appears that the circuit contains both negative and positive feedback. However, overall the system has a positive feedback. To prove that to yourself, assume that there is negative feedback and "virtual short principle" applies, $v_n = v_p$. The only possible solution in this case is if $v_c = v_o = 0$. If $v_c \neq 0$ (even by a small amount, *e.g.,* noise), a voltage difference between v_n and v_p appears and forces the comparator to be saturated.



Resistors R_2 and R_3 act as a voltage divider as $i_p = 0$. Therefore,

$$v_p = \frac{R_2}{R_2 + R_3}\, v_o$$



The RC part acts independently since $i_n \approx 0$ as shown. If at time t_0, a voltage v_o is applied to this circuit and assuming the voltage across the capacitor at this time is $v_c(t_0)$, the capacitor charges according to the following equation:

$$v_c(t) = v_o + [v_c(t_0) - v_o]\, e^{-(t - t_0)/\tau}$$

where $\tau = R_1 C$ is the time constant of the RC circuit.

The method of solution for this circuit is similar to that of Schmidt trigger. Because of positive feedback, the comparator is saturated and $v_o = v_s^+$ (when $v_d > 0$) or $v_o = v_s^-$ (when $v_d < 0$). The two legs of the circuit (RC vs R_2 and R_3) behave differently. If v_o changes suddenly, v_p follows and changes suddenly. However, v_n cannot change suddenly as the voltage across the capacitor has to be continuous. This delay in the response of RC leg is used to make the output signal to oscillate between its two state.

Let's start by assuming that the circuit starts to operate at time $t = 0$, and at that time $v_c(t = 0) = 0$ and $v_0 = +v_s$. The capacitor starts to charge and its voltage increase according to the formula above with $t_0 = 0$, $v_o = +v_s$, and $v_c(t_0) = 0$:

$$v_n = v_c(t) = v_s - v_s e^{-t/\tau}$$

At time $t = 0$, $v_n = 0$ but as time goes on, v_n increases and at some time (call it t_1), it will exceed $v_p = v_s(R_2)/(R_2 + R_3)$ slightly. At a that time v_d becomes negative forcing the comparator output to switch to $-v_s$, which also changes v_p.

At time t_1, $v_o = -v_s$, $v_c(t_1) = v_n(t_1) = (v_s R_2)/(R_2 + R_3)$ and $v_p(t_1^+) = -(v_s R_2)/(R_2 + R_3)$. At this time capacitor is connected to a negative voltage source. It slowly discharges and then begin to charge negatively according to the formula for the RC circuit above with $t_0 = t_1$, $v_o = -v_s$:

$$v_n = v_c(t) = -v_s \left[v_s \frac{R_2}{R_2 + R_3} + v_s \right] e^{-(t - t_1)/\tau}$$

As time goes on, v_n continues to decrease and at some time (call it t_2), it will become smaller that $v_p = (v_s R_2)/(R_2 + R_3)$ slightly. At a that time v_d becomes positive forcing the comparator output to switch to $+v_s$ and the process starts all over again as can be seen in the figure below.

The output signal, v_o is a square wave with an amplitude of v_s (peak to peak of $2v_s$). The period of this square wave, T can be found from

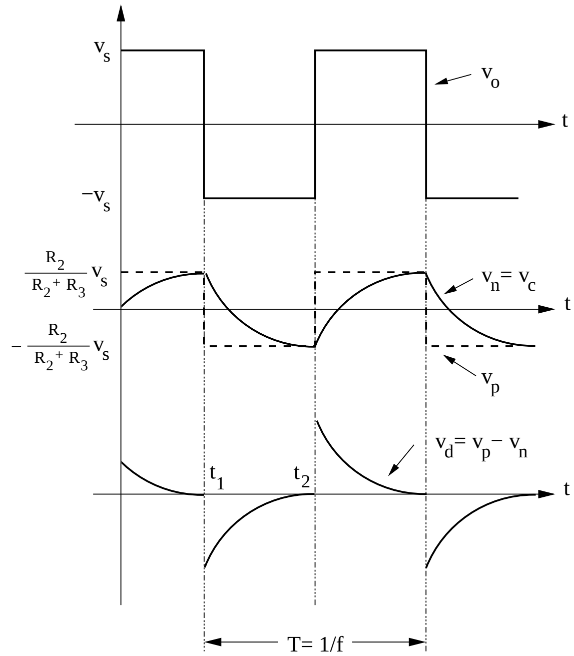
$$T = 2(t_2 - t_1)$$

$$v_n(t_2) = v_c(t_2) =$$

$$= -v_s + \left[v_s \frac{R_2}{R_2 + R_3} + v_s\right] e^{-(t_2 - t_1)/\tau}$$

$$v_p(t_2^-) = -v_s \frac{R_2}{R_2 + R_3}$$

where t_2^- is the time very close to t_2 but still smaller than t_2. comparator switches to other state when $v_n(t_2) = v_p(t_2^-)$. Equating the above expression for $v_n(t_2)$ and $v_p(t_2^-)$, we get:



$$-v_s + \left[v_s \frac{R_2}{R_2 + R_3} + v_s\right] e^{-(t_2 - t_1)/\tau} = -v_s \frac{R_2}{R_2 + R_3}$$

$$\left[\frac{R_2}{R_2 + R_3} + 1\right] e^{-(t_2 - t_1)/\tau} = 1 - \frac{R_2}{R_2 + R_3} = \frac{R_3}{R_2 + R_3}$$

$$e^{-(t_2 - t_1)/\tau} = \frac{R_3}{2R_2 + R_3}$$

$$\frac{t_2 - t_1}{\tau} = \ln\left(\frac{2R_2 + R_3}{R_3}\right)$$

$$T = 2(t_2 - t_1) = 2\tau \ln\left(\frac{2R_2}{R_3} + 1\right) \qquad \tau = R_1 C$$

So this is a square-wave generator. The amplitude of the square wave is set by the saturation voltage of the OpAmp (v_s and $-v_s$) and a period T given by the formula above. The period of this oscillator is controlled mainly by τ as R_2 and R_3 appear inside the log. Typically R_2 and R_3 are chosen in the range of tens of kΩ and of the same magnitude (meaning they are not different by more than a factor of 5).